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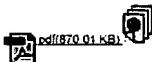
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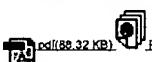
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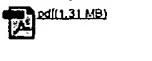
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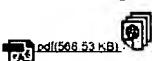
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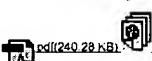
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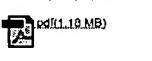
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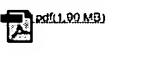
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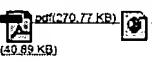
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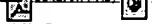
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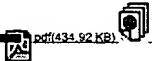
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[Processor Design for Portable Systems - Burd \(1996\) \(Correct\) \(36 citations\)](#)

data encoding and decoding, etc.to specialized **DSP** integrated circuits, which can achieve orders of Technique To Increase Energy Efficiency In Custom **Dsp** lcs (fixed Throughput) Is Architectural I/O interface(s)and system control logic (e.g.**PLD**)Integrated solutions have been developed for infopad.eecs.berkeley.edu/infopad-ftp/papers/1996/Processor_Design_for_Portable_Systems/VLSI_Journal_of_SigProc.ps.gz

[The Future of Reconfigurable Systems - Hauck \(1998\) \(Correct\) \(1 citation\)](#)

chip, requiring the integration of FPGAs with CPUs, **DSPs**, and SRAMs. Reconfigurable computing specific this demands the inclusion of microprocessor, **DSP**, and SRAM resources. In future reconfigurable the low-end FPGA market itself is being eroded by **PLDs** and embedded processors. This is particularly www.ee.washington.edu/faculty/hauck./publications/ReconfigFuture.PDF

[Simulation of Evolvable Hardware to Solve Low Level.. - Hollingworth.. \(1999\) \(Correct\) \(1 citation\)](#)

is simple to implement on Digital Signal Processor(**DSP**) technology. The first step in testing Image (FPGA)7] devices and Programmable Logic Devices (**PLD**)since these can be programmed using a binary www.amp.york.ac.uk/external/media/cal/bio-insp/publications/gsh-evoiasp99.pdf

[FPGA based RF control - Burghardt Askon Beratungs \(2003\) \(Correct\)](#)

- mentsation features digital signal processors (**DSP**) for computing and processing the necessary Despite the fact, that the selected 320TMS6701 **DSPs** from TI contain four parallel execution units, in the field of programmable logic devices (**PLD**)They have a long and successful history since tesla.desy.de/new_pages/TESLA_Reports/2003/pdf_files/tesla2003-16.pdf

[A DSP-Based Platform for Wireless Video Compression - Patrick Murphy Vinay \(2002\) \(Correct\)](#)

1 A **DSP**-Based Platform for Wireless Video Compression

paper describes a modular and standards-independent **DSP**-based testbed (Paladin) designed for real-time Transceiver Cmos Imager (cif/qcif) Fifo 1kx16) **PLd** Fifo 2kx8) 16-Bit 16-Bit Control 8-Bit 8-Bit cmc.rice.edu/docs/docs/Mur2002Nov5ADSP-Based.pdf

[Active SANs: Hardware Support for Integrating.. - Ulmer, Wood.. \(Correct\)](#)

in the local host. In [5] researchers place FPGA, **DSP**, and ATM cards in a host to enhance node hardware is a programmable logic device (**PLD**)An example of such a device is a Field www.csl.cornell.edu/SAN-1/craig.pdf

[Reconfigurable Computing In Communications Systems - Tommiska \(1998\) \(Correct\)](#)

Figure 19 AT6010 as a **DSP** Coprocessor

Standard DPGA Dynamically Programmable Logic Array **DSP** Digital Signal Processing, Digital Signal PL Priority Level PLA Programmable Logic Array **PLD** Programmable Logic Device QoS Quality of Service wooster.hut.fi/~matti/lisuri.pdf

[>100 ---- - In In In \(Correct\)](#)

-32-Bit) Mms T800 Cmos Inm -32-Bit) A We-**Dsp**32c **Dsp** Cmos Att -J 320c25 **Dsp** Tix -france) Mms T800 Cmos Inm -32-Bit) A We-**Dsp**32c **Dsp** Cmos Att -J 320c25 **Dsp** Tix -france) Jh Normal Incidence, Having An Let=36 To 40 Esa Ep600 **PLd** -Alt -Esa 2ora1oz **PLd** -Gdd 22vi Oc-1 techreports.jpl.nasa.gov/1993/93-1237.pdf

[Tradeoff Analysis of Integer Multiplier Circuits.. - Thornton, Gaiche.. \(Correct\)](#)

of general arithmetic and digital signal processing (**DSP**) circuitry [4] 2]DSP processing tasks have digital signal processing (**DSP**) circuitry [4] 2]DSP processing tasks have traditionally been realized to a sample of modern Programmable Logic Devices (**PLDs**)Although it is generally accepted that superior www.ece.msstate.edu/~mitch/pubs_dir/../ftp_dir/pubs/pacrim99-2.ps

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Conceptual Prototyping Of Scalable Embedded Dsp Systems Lan-Rong Dung Georgia Institute Of Optimization in Register-Transfer Scheduling for DSPSystems, Proc. ACM/IEEE Design Automation Conf. Ehitajate tee 5, EE-0026 Tallinn, Estonia raiub@pld.ttu.ee. Test Synthesis with Alternative Graphs www.iro.umontreal.ca/~aboulham/synthA97.pdf

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